

WHAT IS CLAIMED IS:

1           1.    A method of manufacturing an integrated circuit, the method  
2    comprising:  
3                providing a gate dielectric layer above a top surface of a  
4    substrate;  
5                providing a silicon and nitrogen containing layer above the  
6    gate dielectric layer;  
7                providing an oxide layer above the silicon and nitrogen  
8    containing layer;  
9                selectively etching the oxide layer to form a first trench in  
10   the oxide layer;  
11               selectively etching the silicon and nitrogen containing layer  
12   to form a second trench in the silicon and nitrogen containing layer, the  
13   second trench being narrower than the first trench and being disposed  
14   below the first trench; and  
15               providing a gate conductor material in the first trench and  
16   the second trench.

1           2.    The method of claim 1, further comprising removing the  
2   oxide layer.

1           3.    The method of claim 2, further comprising:  
2                removing portions of the silicon and nitrogen containing  
3   layer, whereby a pair of spacers remain underneath the gate conductor  
4   material in the first trench.

1           4.    The method of claim 3, wherein the gate conductor material  
2   is removed by a polishing process.

1           5.     The method of claim 3, wherein the silicon and nitrogen  
2 containing layer includes silicon rich nitride.

1           6.     The method of claim 1, wherein the selective etching the  
2 silicon and nitrogen containing layer includes a RELACS process.

1           7.     The method of claim 1, wherein the silicon and nitrogen  
2 containing layer includes SiON or silicon rich nitride.

1           8.     The method of claim 7, wherein the silicon and nitrogen  
2 containing layer is a silicon rich nitride layer.

1           9.     The method of claim 1, wherein a width of the first trench is  
2 at least 250 Å and less than 1600 Å.

1           10.    The method of claim 9, wherein the width of the second  
2 trench is at least 400 Å and less than 2100 Å.

1           11.    A method of manufacturing an ultra-large scale integrated  
2 circuit including a transistor with a T-shaped gate conductor, the method  
3 includes steps of:

4                   providing a first layer above a substrate, the first layer being  
5 a silicon rich nitride layer or a silicon oxynitride layer;

6                   providing an oxide layer over the first layer;

7                   forming a first trench in the oxide layer;

8                   forming a second trench in the first layer, the second trench  
9 having a smaller width than the first trench; and

10                  providing a gate conductor material in the first trench and in  
11 the second trench to form the T-shaped gate conductor.

1           12.    The method of claim 11, further comprising removing the  
2 oxide layer.

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1 13. The method of claim 12, further comprising removing  
2 portions of the first layer to leave spacers underneath the gate conductor  
3 material in the first trench, the removal process utilizing the gate  
4 conductor material as a mask.

1 14. The method of claim 13, wherein the first layer is silicon rich  
2 nitride.

1 15. A method of manufacturing a gate conductor for an  
2 integrated circuit, the method comprising:  
3 providing a first layer above a gate dielectric layer, the gate  
4 dielectric layer being above a substrate, the first layer including silicon  
5 oxynitride or silicon rich nitride;  
6 forming an aperture in the first layer utilizing a RELACS  
7 process;  
8 filling the aperture with a gate conductor material; and  
9 removing the gate conductor material above the first layer.

1 16. The method of claim 15, further comprising:  
2 providing an oxide layer above the first layer and forming an  
3 aperture in the oxide layer before forming the aperture in the first layer.

SUB B3 1 17. The method of claim 16, wherein the gate conductor material  
2 is doped or undoped polysilicon material.

1 18. The method of claim 17, wherein a T-shaped gate conductor  
2 is formed.

SUB A2 1 19. The method of claim 16, wherein the gate conductor material  
2 is also provided in the aperture in the oxide layer.

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20. The method of claim 16, wherein the oxide layer is silicon dioxide.

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